IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of

COKER et al — Atty. Ref.: 124-865

Serial No. 09/868,242 — Group: 2674

Filed: January 10, 2002 — Examiner: R. Laneau

For: FAST READOUT OF MULTIPLE DIGITAL BIT PLANES FOR DISPLAY OF GREYSCALE IMAGES

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APPEAL BRIEF

On Appeal From Group Art Unit 2674

Stanley C. Spooner
NIXON & VANDERHYE P.C.
8th Floor, 1100 North Glebe Road
Arlington, Virginia 22201-4714
(703) 816-4028
Attorney for Appellant

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CLAIMS APPENDIX A1

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Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified appeal is QinetiQ Limited by virtue of an Assignment of rights from the inventors to the Secretary of State for Defence recorded January 10, 2002 at Reel 12500, Frame 0001 and a subsequent Assignment from the Secretary of State for Defence to QinetiQ Limited recorded February 20, 2002 at Reel 12831, Frame 459.

II. RELATED APPEALS AND INTERFERENCES

There are believed to be no related appeals, interferences or judicial proceedings with respect to the present application and appeal.

III. STATUS OF CLAIMS

Claims 1-3, 7 and 9-11 stand rejected in the outstanding Official Action. The Examiner contends that claims 1-3, 7 and 9-11 are obvious in view of the cited prior art references under 35 USC §103 as set forth in the second non-final Official Action.

IV. STATUS OF AMENDMENTS

No further response has been submitted with respect to the second non-final Official Action in this application.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention relates to a method of addressing a display, such as a spatial light modulator, with an array of binary pixels and in particular a display device such as a liquid crystal display that has pixels that are switchable between a transmissive (white) and non-transmissive (black) states.

It is well known that such displays can be operated in gray scale by varying the amount of time that each pixel spends in the black and white states. It is also

known to address each pixel by a weighted bit plane technique where the pixel is addressed in a series of sub-frames, each of a different duration. The addressing signal for each sub-frame is the bit-plane. Thus, in a simple example where a pixel is addressed in three frames of duration 4t, 2t and t, respectively, a total of 8 gray scale levels can be achieved. The addressing signal would then be a 3-digit binary number with, for example, 1 representing the white state and 0 representing the black state. Thus, 000 would be all black (or gray level 0), 111 would be all white (or gray level 7) and 101 would be gray level 5 (in all cases where the most significant bit is first).

Where there are a plurality of pixels, the most significant bits for each pixel may form a binary string or a "first bit plane", the next most significant bits forming a second binary string or "second bit plane", and so on. Again, by way of example, a display comprising four pixels, for which the relevant gray levels are respectively gray level 2 (010), gray level 4 (100), gray level 5 (101) and gray level 1 (001), the most significant bits of each of these four form a first binary string or bit plane A (0, 1, 1, 0). The next most significant bits form a second string or bit plane B (1, 0, 0, 0) and the least significant bits form a third string or bit plane C (0, 0, 1, 1).

Thus, addressing data may form three separate binary strings or bit planes A, B, C. If the display is such that the pixel can adopt the required display state for the required duration, then the addressing signal needs only to be applied once

at the appropriate time. However, in some displays, especially liquid crystal displays utilizing thin film transistors, the data needs to be refreshed during the longer duration sub-frames. The refresh level may be the period for which the least significant (or lowest weighted) bit plane is applied, i.e., for the period t in the example above.

Therefore, in order to be able to obtain the required image exposure where the three frames of duration are 4t, 2t and t, bit plane A would be written four times (4t duration), bit plane B twice (2t duration) and bit plane C once (t duration), i.e., AAAABBC. As discussed on amended sheet page 7, lines 6-10, reading out the bit planes in this order would necessitate storing the start address of each binary string or bit plane in memory for readout the necessary number of times.

Appellants found that a significant improvement can be made by storing the binary strings or bit planes in memory in order of decreasing weighting, i.e., in order A, B and C. The Appellants then readout the bit planes from the beginning a repeated number of times, i.e., the first time the entire string is readout, i.e., A, B, C. However, after this first readout, bit plane C has already been readout for the total correct period of time. Therefore, the number of strings to be readout is reduced by 1 so that for the next frame the readout step only reads out bit planes A and B. After this readout, bit plane B has been readout the correct number of

times, so the number of strings to be readout is reduced again. Bit plane A is therefore readout twice to complete the readout cycle.

As a result, the actual readout sequence would be ABCABAA. In view of the above, the advantage of the present invention is apparent. Only one start location is required to be stored in memory, the number of strings of bit planes to be readout are simply determined by a counter as discussed in Appellants' specification page 9, lines 19-24. The benefit, of course, is that because only the start address need be stored to access a particular bit plane and counters keep track of the number of times the bit plane has been read, the amount of active storage is effectively reduced.

Thus, the present invention is claimed in independent claims 1 and 11. Claim 1 more broadly recites a method of image signal processing whereas claim 11 recites a method of displaying an image. In both instances, a plurality of binary strings of data defining a multi-level image is stored in a memory where the strings have respective weightings and define respective bit planes and each bit plane corresponding to a digitized pixelwise intensity distribution. In claim 1, the method comprises the steps of "**storing the strings in sequential locations in said memory in decreasing order of weighting**," and "**making a succession of read cycles from the stored strings**" where each read cycle consists of first "**reading at least one of the stored strings** in sequence as stored, **commencing with the string for the highest weighting**" and, secondly, "**the numbers of the**

strings read in the read cycles being varied so that at the end of the succession of read cycles **each string has been read out a number of times proportional to its associated weighting**."

Claim 11 is limited in the manner of claim 1 and further limited in that each "**binary string [is] representing a weighted bit plane for display**" and has a "**number of read out times associated therewith**". The final step also includes "**reading out each sequential stored binary string which has not yet been read out the appropriate number of read out times**."

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3, 7 and 9-11 stand rejected under 35 USC §103 as unpatentable over Strohacker (U.S. Patent 6,320,986) in view of Gale et al (U.S. Patent 5,737,038) and further in view of Doherty et al (U.S. Patent 5,657,099).

VII. ARGUMENT

Appellants arguments include the fact that the burden is on the Examiner to demonstrate where at least one reference in a combination of references teaches or suggests each of the method steps recited in independent claims 1 and 11. Additionally, even if the method steps are shown in a group of prior art references, there must be some reason or motivation to combine the references in the manner of method claims 1 and 11. Finally, the primary reference, by the Examiner's own

admission, teaches away from the claimed invention, thereby rendering unsupported any obviousness rejection.

1. No references teach or suggest the combination of claimed steps "storing" and "making"

(a) Claims 1-3, 7, 9 and 10

Independent claim 1 specifies a method of image signal processing with a signal defining a pixellated multi-level image where the processing method comprises the steps of "storing said strings in sequential locations in said memory in decreasing order of weighting" and the step of "making a succession of read cycles from the stored strings" wherein each read cycle has the step of reading the strings in the "sequence as stored" and "commencing with the strings for the highest weighting" and the number of the strings read in the read cycles "being varied" so that at the end of the succession of read cycles "each string has been read out a number of times proportional to its associated weighting."

The Court of Appeals for the Federal Circuit has consistently held that "the PTO has the burden under §103 to establish a *prima facie* case of obviousness." *In re Fine,* 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). The Court went on to indicate that the PTO "can satisfy this burden only by showing some objective teaching in the prior art . . . ." Thus, in accordance with the controlling Federal Circuit decision, Appellants' claimed sequence of steps, either separately or together, must be shown somewhere in at least one of the three cited prior art references.

The Examiner admits that "Strohacker does not teach binary strings associated with the highest weightings stored in memory" (section 5, page 3 of the Official Action). In addition to the Examiner's admission, a review of the Strohacker reference clearly indicates that it contains no teaching about how the reading out of bit planes or binary strings is to be done, let alone in a series of read-out cycles, each starting with the most significant bit. In fact, Strohacker is not believed to contain any teaching regarding how stored data is to be read out let alone the claimed read out method.

The Examiner's reference to Gale et al as suggesting special data sequences regarding the order of display times is not an allegation that Gale teaches the missing Strohacker teaching, i.e., storage of binary strings associated with the highest weightings stored in memory or any read-out of data stored. So there is no allegation that Gale supplies the missing teaching.

The Gale reference teaches a method of reducing artifacts in a displayed image by varying when differently weighted bit planes are applied for the differently colored pixels. Figure 3 of Gale shows a conventional approach where a frame consists of bit planes 2, 1 and 0 in decreasing order of weighting and shows the red, green and blue pixels all being addressed at the same time. Apparently, this arrangement leads to image artifacts so that in one embodiment (Figure 4), Gale teaches that the bit planes for each pixel are staggered with

respect to one another and in another embodiment (Figure 5), the order of writing is changed for each colored pixel.

Therefore, Gale clearly teaches that storage in decreasing order of weighting causes "image artifacts" and this is the problem solved by the Gale reference. Clearly, Gale teaches away from any method whereby bit planes are read out in order of decreasing weighting in a number of read-out cycles. Moreover, the embodiment shown in Figure 4 has only a single read-out cycle, not a "succession of read cycles from the storage strings" as required by independent claim 1.

The Examiner admits that "neither Strohacker not [sic] Gale teaches a method whereby bit planes are read out in order of decreasing weighting" and this admission is very much appreciated. The Examiner suggests that Doherty supplies the missing teaching from Strohacker and Gale and concludes that Doherty teaches a bit memory that operates as a first-in, first-out buffer. However, this is not an allegation that Doherty supplies the method step missing from Strohacker and Gale, i.e., "bit planes are read out in order of decreasing weighting."

Thus, it is clear that the Examiner admits that the subject matter of claim 1, i.e., "bit planes are read out in order of decreasing weighting," is not taught in the Strohacker and Gale references, and the Examiner fails to indicate how or where the Doherty reference contains the missing teaching.

In fact, none of the prior art references teaches storing strings in decreasing order of weighting and then making "a succession of read cycles" from the stored strings. Moreover, the Examiner appears to have ignored the further language in Appellants' independent claim 1 which states that the numbers of strings read out in the read cycles are varied so that at the end of the read cycles "each string has been read out a number of times proportional to its associated weighting."

As noted in *In re Fine*, the burden is on the Examiner to show that the claimed method steps are at least disclosed in one of the three cited references. However, the Examiner has identified no language in any of the references that discusses that the number of strings read in the read cycle can be varied so that "each string has been read out a number of times proportional to its associated weighting." Importantly, the Examiner admits that this teaching is missing from the Strohacker and Gale references and fails to disclose where the Doherty reference contains any such teaching.

As a result of the above, the Examiner has simply failed to meet his burden of proof with respect to the rejection of claims 1-3, 7, 9 and 10 under 35 USC §103 over the Strohacker/Gale/Doherty combination of references.

(b) Claim 11

Independent claim 11 is a somewhat narrower claim than independent claim 1 and is limited to a method displaying an image on a pixellated display.

While this method would fall within the scope of independent claim 1, claim 11, not only includes the limitations of claim 1, but more specifically recites the particular read-out cycles. Inasmuch as claim 11 incorporates the limitations of claim 1 which the Examiner admits are not present in Strohacker and Gale and which the Examiner fails to disclose being taught in Doherty, the above arguments with respect to claim 1 are directly applicable to independent claim 11 and therefore those arguments are herein incorporated by reference.

Claim 11 more specifically recites in step (i) that "the number of read out times is proportional to the weighting of the bit plane," and in step (iii) "repeatedly reading out binary strings in a plurality of read out cycles" where each cycle starts "with the binary string according to the highest weighting bit plane and reading out each sequential stored binary string which is not yet been read out the appropriate number of read out times." Again, these details of independent claim 11 are not alleged or suggested to have been disclosed in either Strohacker or Gale or Doherty.

As a result, the Examiner has not met his burden of proof of establishing that any one of the prior art references or any combination of the prior art references discloses each of the claimed method steps set out in Appellants' independent claim 11. Therefore, the rejection under 35 USC §103 is not properly supported.

2. The Examiner fails to identify any motivation or reason to combine the three prior art references

The Examiner combines the Strohacker reference, the Gale reference and the Doherty reference in order to suggest that independent claims 1 and 11 and claims 2, 3, 7, 9 and 10 (dependent on claim 1) are obvious.

The Court of Appeals for the Federal Circuit has held in the case of In re Rouffet, 47 USPQ2d 1453, 1457-8 (Fed. Cir. 1998) that

> "to prevent the use of hindsight based on the invention to defeat patentability of the invention, **this court requires the examiner** to show a motivation to combine the references that create the case of obviousness. In other words, **the Examiner must show reasons** that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." (emphasis added).

On page 4 of the Official Action, the Examiner merely concludes that it "would have been obvious to one of ordinary skill in the art" to utilize portions of the Gale and Strohacker references and then combine those with a possible read-out technique taught by Doherty. The Examiner has provided no "motivation" or "reason" for one of ordinary skill in the art, without knowledge of the claimed invention, to select the method steps disclosed in the Strohacker, Gale and Doherty references.

Because the burden is on the Examiner (in order to prevent the prohibited use of hindsight) to show both a motivation and a reason for combining, and because the Examiner has failed to meet this burden, even if the Strohacker, Gale

and Doherty references taught Appellants' claimed method steps (which as noted above is not taught), the Examiner has failed to meet the burden under *In re Rouffet* of showing that the Examiner did not use prohibited hindsight in his combination rejection.

As a result, independent claims 1 and 11 and claims 2, 3, 7, 9 and 10 dependent on claim 1 are clearly patentable over the Strohacker/Gale/Doherty combination.

3. The primary reference actually teaches away from the claimed invention

The Court of Appeals for the Federal Circuit has also consistently held that it is "error to find obviousness where references 'diverge from and teach away from the invention at hand'." *In re Fine*, at 1599.

The Examiner admits that in Strohacker, "Figure 5 shows an example of a binary string from the least significant bit to the most significant bit." Thus, if Strohacker were adopted, any binary string stored in memory as per the Doherty reference would be stored from the least significant bit to the most significant bit. This is precisely the opposite of Appellants' claimed requirement in claims 1 and 11 that the strings be stored "in decreasing order of weighting." Thus, Strohacker, the primary reference, would lead one of ordinary skill in the art away from Appellants' invention.

As noted by the Federal Circuit, it is error for the Examiner to conclude independent claims 1 and 11 (and claims dependent on claim 1) are obvious where Strohacker teaches away from the claimed invention.

VIII. CONCLUSION

Appellants have demonstrated that the single rejection of all pending claims is based upon a combination of three individual references. The Examiner has admitted that two of the references fail to teach a claimed structure, but the Examiner fails to point out where the third reference actually teaches the missing method steps. Apart from failing to teach all claimed method steps, the Examiner also fails to point out how or where there is any motivation or suggestion for combining the references. Finally, the Examiner acknowledges that the primary reference teaches the direct opposite of Appellants' claimed combination of method steps, but apparently does not believe this defect would actually lead those of ordinary skill away from the reference at hand.

Thus, and in view of the above, the rejection of claims 1-3, 7 and 9-11 under 35 USC §103 is clearly in error and reversal thereof by this Honorable Board is respectfully requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____

Stanley C. Spooner
Reg. No. 27,393

SCS:kmm
Enclosures
Appendix A - Claims on Appeal

CLAIMS APPENDIX

1. A method of image signal processing wherein a signal defining a pixellated multi-level image is defined by a first plurality of binary strings in a memory, the strings having associated therewith respective weightings and defining respective bit planes each bit plane corresponding to a digitised pixelwise intensity distribution, such that the weighted pixelwise intensity distribution over all said plurality of bit planes corresponds to said multi-level image, comprising the steps of:

storing said strings in sequential locations in said memory in decreasing order of weighting; and

making a succession of read cycles from the stored strings, each read cycle consisting of

reading at least one of the stored strings in sequence as stored, commencing with the string for the highest weighting,

the numbers of the strings read in the read cycles being varied so that at the end of the succession of read cycles each string has been read out a number of times proportional to its associated weighting.

2. A method according to claim 1 wherein the multi-level image is a multi-intensity image.

3. A method according to claim 1 or claim 2 wherein the said succession of read cycles is repeated.

7. A method of imaging comprising the steps of performing the method according to claim 1 and displaying each string as a bit plane each time each string is read during the succession of read cycles for substantially the same period.

9. A method of imaging according to claim 7, wherein the bit planes are displayed on a pixellated liquid crystal display.

10. A method according to claim 9 wherein a small ac potential difference is applied to pixels of the display in periods when bit planes are not being written.

11. A method of displaying an image on a pixellated display using a weighted bit plane technique, the method involving the steps of:

(i) defining a plurality of binary strings, each binary string representing a weighted bit plane for display and having a number of read out times associated therewith, the number of read out times proportional to the weighting of the bit plane,

(ii) storing said binary strings in a display memory in sequential order of decreasing weighting of bit plane, and

(iii) repeatedly reading out the binary strings in a plurality of read out cycles, each cycle starting with the binary string according to the highest weighting bit plane and

reading out each sequential stored binary string which has not yet been read out the appropriate number of read out times.